BT258S-800R

Logic level thyristor

20 March 2014 **Product data sheet**

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT428 (DPAK) surface mountable plastic package intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct interfacing with low power drivers and microcontrollers
- High bidirectional blocking voltage capability
- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate suitable for logic level controls
- Surface mountable package

3. Applications

- General purpose switching and phase control
- Protection circuits
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
V_{RRM}	repetitive peak reverse voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	75	A
T_j	junction temperature		[1]	-	-	125	°C
$I_{T(RMS)}$	RMS on-state current	half sine wave; T_{mb} ≤ 111 °C; Fig. 2; Fig. 3		-	-	8	A

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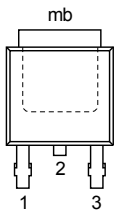
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 8		-	50	200	µA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 13		50	100	-	V/µs

[1] Operation above junction temperatures of 110 °C may require the use of a gate to cathode resistor of 1 kΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 **DPAK (SOT428)**	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT258S-800R	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

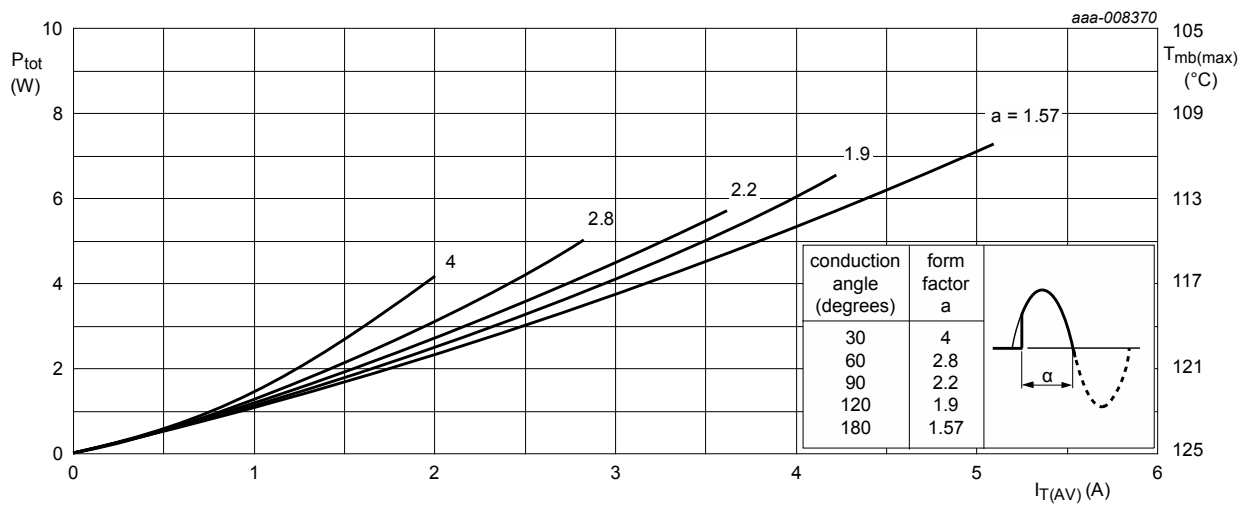
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
V_{RRM}	repetitive peak reverse voltage			-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111$ °C; Fig. 1		-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111$ °C; Fig. 2; Fig. 3		-	8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	75	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	82	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	28	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 10$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature		[1]	-	125	°C

[1] Operation above junction temperatures of 110 °C may require the use of a gate to cathode resistor of 1 kΩ



a = Form factor = $I_{T(RMS)}/I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values

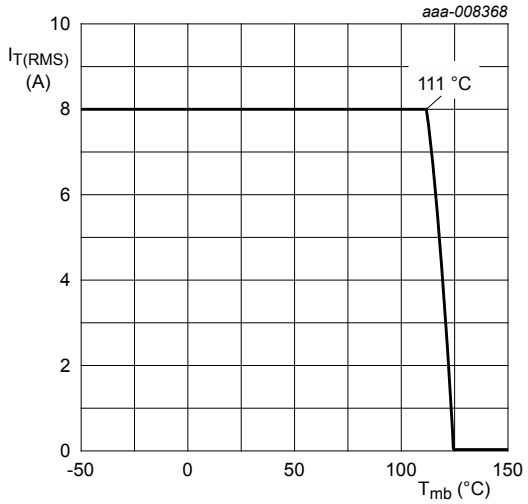
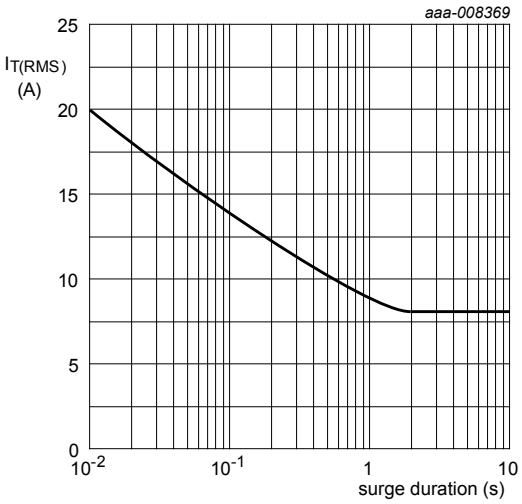
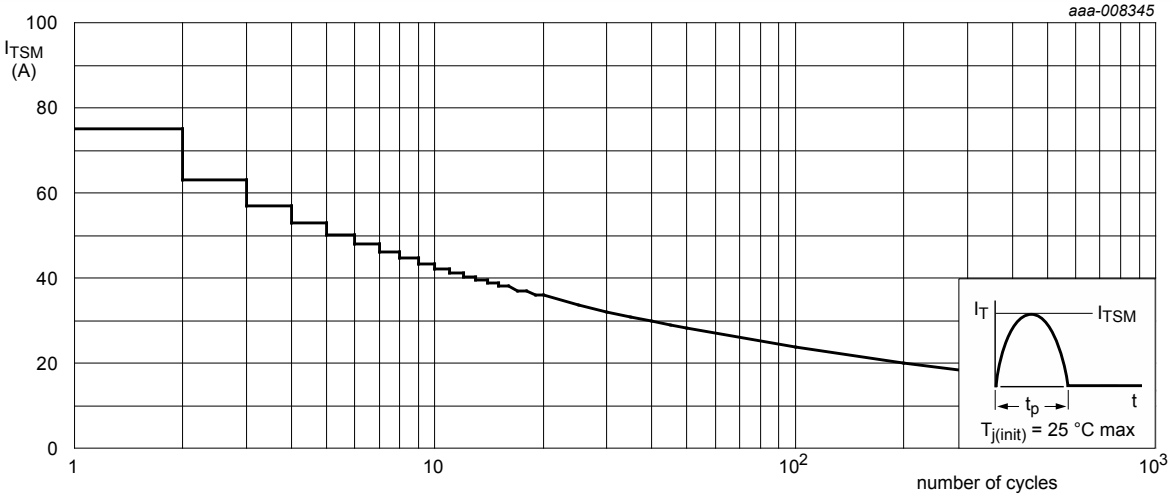


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



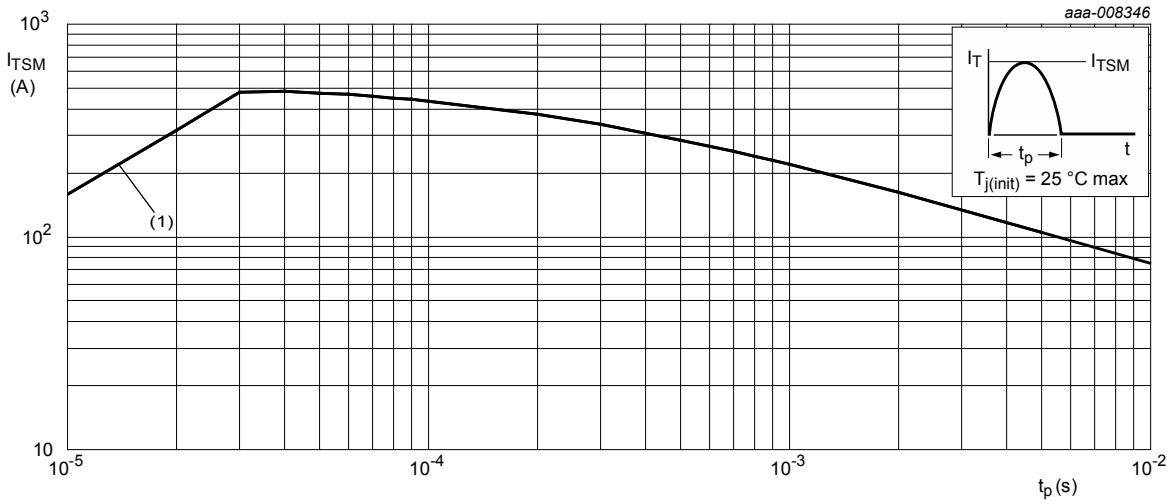
f = 50 Hz; T_{mb} = 111 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Device mounted on an FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint; Fig. 7		-	75	-	K/W

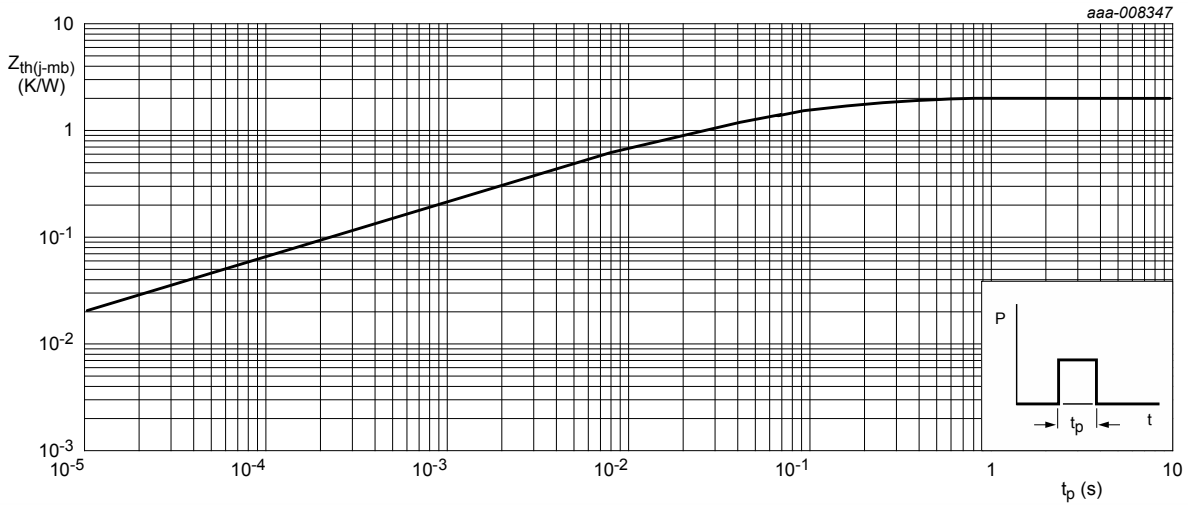
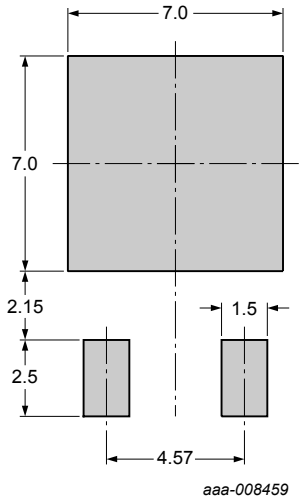


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width



All dimensions are in mm

Plastic meets requirements of UL94 V-O at 3.175 mm

Fig. 7. SOT428: minimum pad sizes for surface-mounting

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 8		-	50	200	µA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 9		-	0.4	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	0.3	6	mA
V_T	on-state voltage	I_T = 16 A; T_j = 25 °C; Fig. 11		-	1.3	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 12		-	0.4	1	V
		V_D = 800 V; I_T = 0.1 A; T_j = 110 °C; Fig. 12		0.1	0.2	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 800 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 13		50	100	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 10 A; V_D = 800 V; I_G = 5 mA; dI_G/dt = 0.2 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 536 V; T_j = 125 °C; I_{TM} = 12 A; V_R = 24 V; $(dI_T/dt)_M$ = 10 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	µs

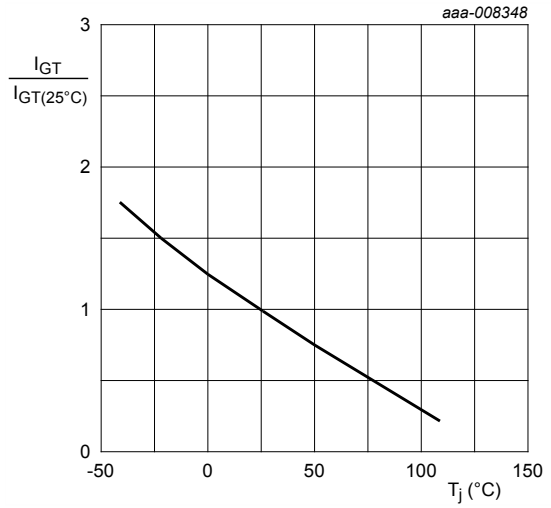


Fig. 8. Normalized gate trigger current as a function of junction temperature

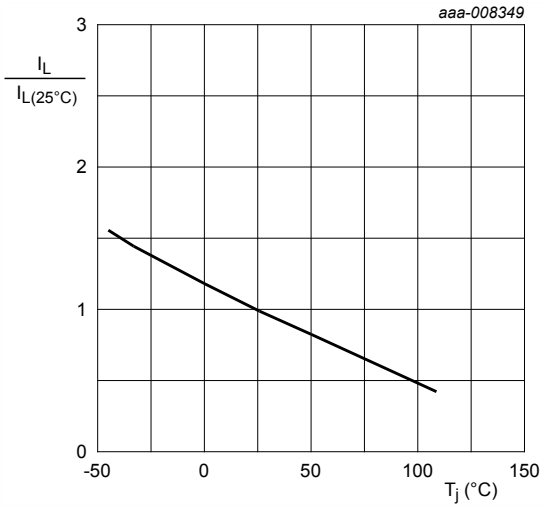


Fig. 9. Normalized latching current as a function of junction temperature

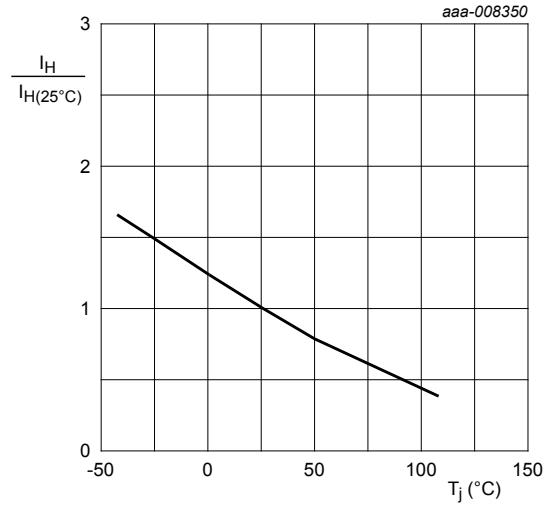
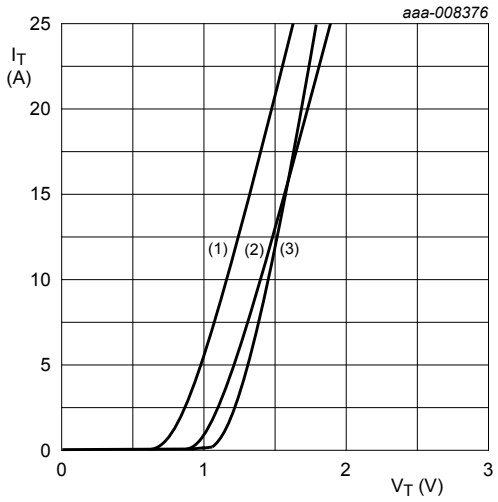


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.0 V; R_s = 0.04 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

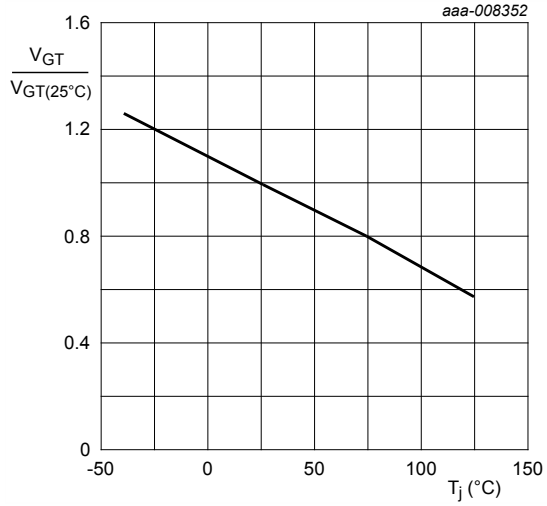
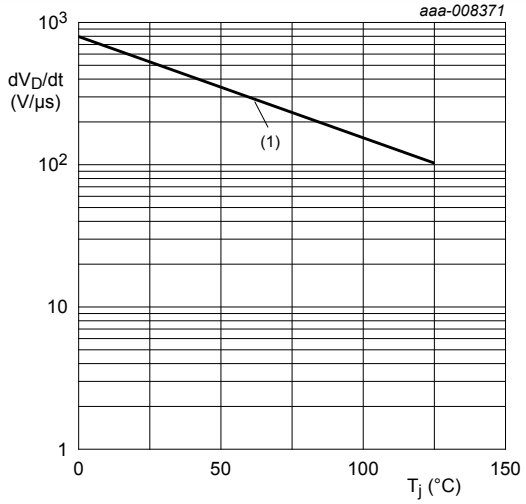


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

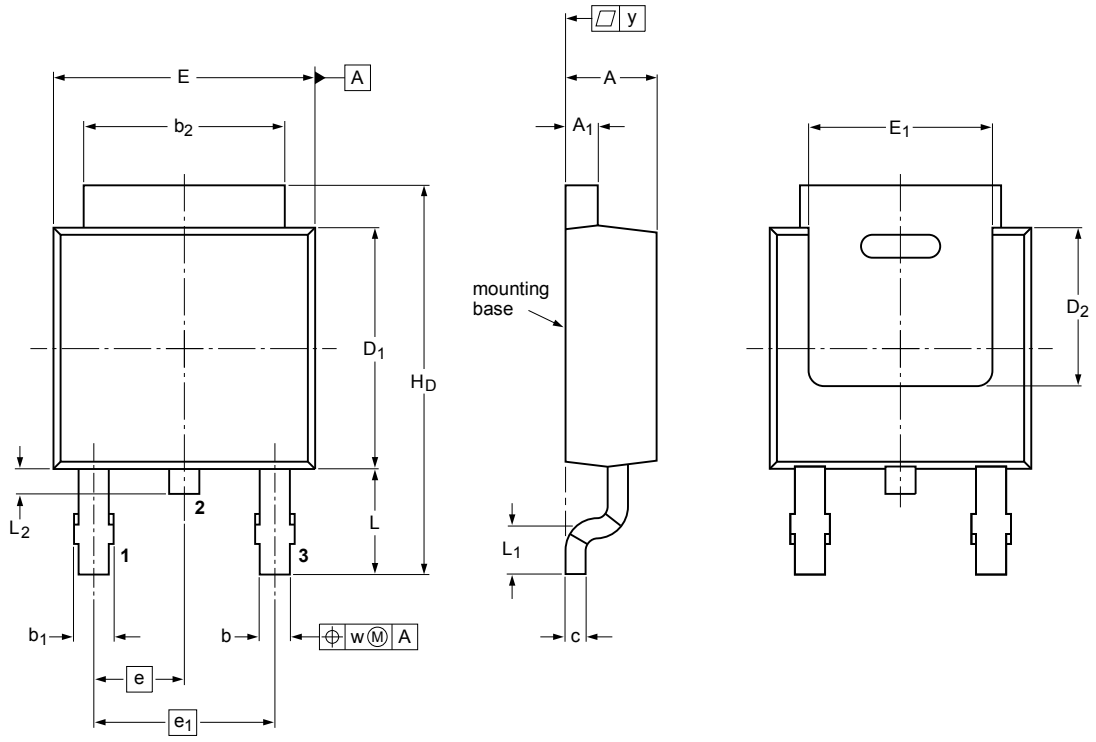


(1) R_{GK} = 100 Ω

Fig. 13. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig. 14. Package outline DPAK (SOT428)

11. Soldering

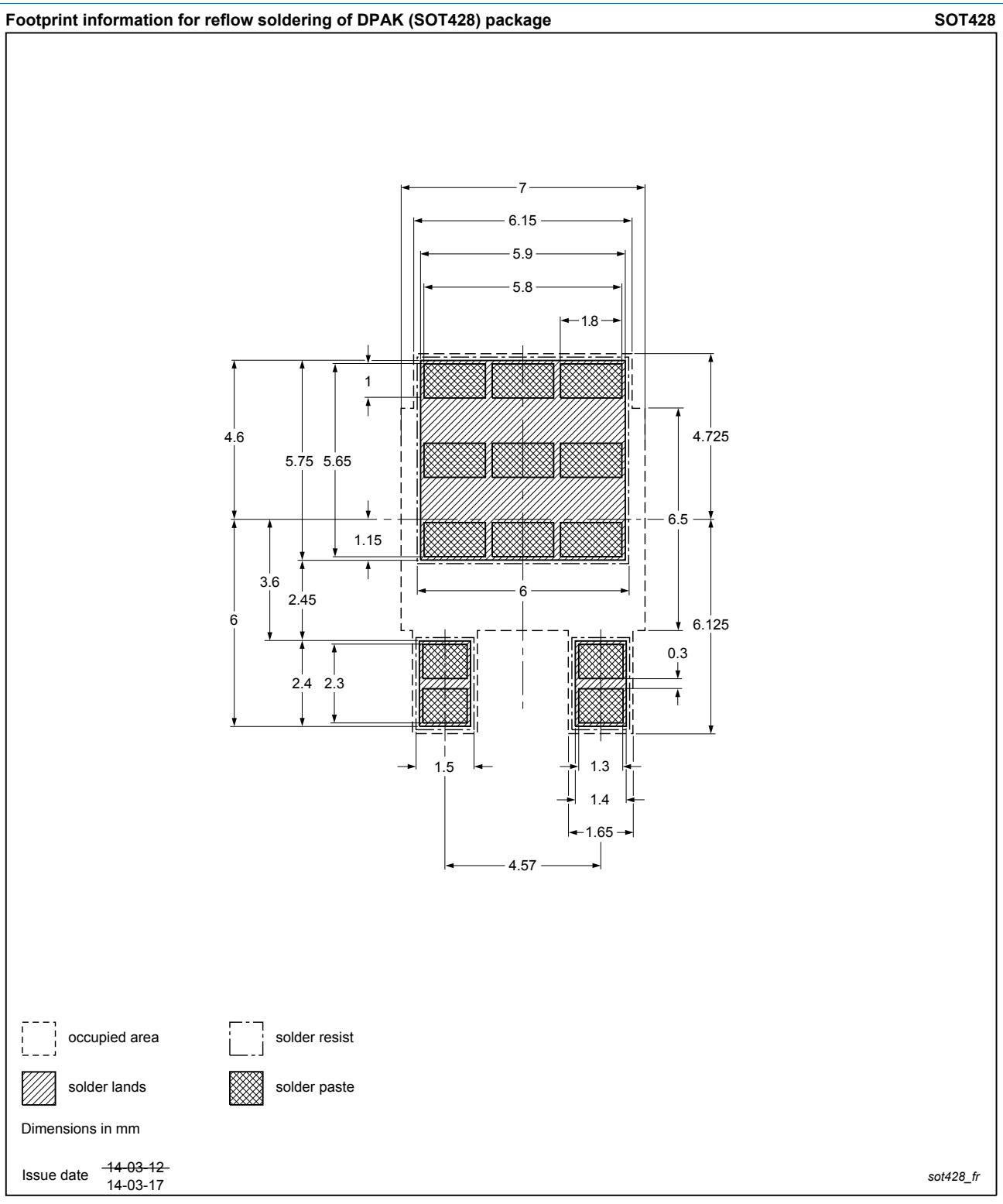


Fig. 15. Reflow soldering footprint for DPAK (SOT428)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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